Power-Device Packaging Beats The Heat

Through Various Thermal Enhancements, Power Packages Strive To Keep Pace With The Growing Power Dissipation Of The ICs They Encapsulate.

DAVID MALINIAK

In the world of semiconductor packaging, most of the attention is focused on high-lead-count digital and mixed-signal ICs. But the real workhorses in most systems are the power devices that fuel those flashy CPUs and DSP ICs. Only a few years ago, it was unheard of for power semiconductors to dissipate much more than half a watt. But the increasing integration of power transistors, coupled with rapidly rising switching frequencies, has brought the power-dissipation issue to a boil, with many devices dissipating several watts or more. The drive to squeeze such hot-running power semiconductors into ever-smaller packages has made for many technical challenges.

For power packaging, the name of the game is power dissipation. Without good thermal management at the level of package design, power devices are easily burned up, even if you practice good thermal management at the system-design level. A number of factors come into play, not the least of them being a balance between the number of leads dedicated to signal duty and leads dedicated to heat removal. The overall package configuration is a major determinant in its ability to dissipate heat.

Two major trends in power packaging have emerged in recent years. One concerns larger chips going into packages with more pins. Witness the fact that the venerable TO-220 power package has grown from a three-leaded package to one with five, then seven leads. This is a direct consequence of the increasing complexity of power devices. Looking back to perhaps the mid-1980s, power devices were basically discrete transistors. Many vendors have long since begun integrating high-density logic along with those transistors. Hence the need for more I/O in power packages.

SURFACE MOUNTING MAKING INROADS

The more important trend, however, is the move from through-hole to surface-mount technology (SMT). According to Mike Hundt, director of corporate packaging development, USA Group, SGS-Thomson Microelectronics, Carrollton, Texas, there are a number of reasons for this trend. "When you have a through-hole part and have to clip or screw it to the wall of the enclosure, there are a number of assembly operations involved there. SMT is done in the same manner as the rest of the on-board parts," Hundt says. Moving power packages from through-hole to SMT configurations required one of several major changes: The conversion from a traditional power lead frame with leads on one side only to lead frames with leads on at least two sides.

Still, says Hundt, the evolution to SMT in power ICs is about 10 years behind that of small-signal ICs. SMT packages remain a distinct minority in power ICs. What drives the move to SMT? First, it's the desire for more efficient manufacturing. Second, it's the on-going effort to miniaturize end products. Finally, there's the issue of reliability. The SMT power packages are generally more reliable than their through-hole predecessors, says Hundt.

The increased reliability for SMT power packages stems from the fact that solder joints tend to be more reliable in the long term than screws and clips.

"Reliability is a matter of how well you can control variation in manufacturing," says Hundt. "There's so much industry experience and expertise in soldering that it's not difficult to get repeatable, high-quality solder joints." That repeatability is harder to achieve when bolting heat tabs to enclosure walls or cold plates. Solder joints are less likely to shake loose than screws. And generally, smaller packages are subject to lower internal stresses than are larger ones.

In designing power packages, there are many materials issues related to the composition of the lead frame itself, the molding compound, and whether to incorporate thermal enhancements such as heat slugs and spreaders. Without adequate thermal management in the package design, the end user is obviously placed at an extreme disadvantage in terms of reliability. Power devices run at much higher junction temperatures than do small-signal devices. According to Mohammed Kasem, senior manager of corporate packaging development and manufacturing engineering at Temic/Siliconix, Santa Clara, Calif., power cycling can cause a large difference between the junction and ambient temperatures. This temperature differential can dramatically affect the package's reliability.

A power device in the wrong package is prone to a number of catastrophic failure modes, some of which can be quite spectacular. These include die cracking, die-attach degradation, and delamination between the package and chip surface. In some cases, the latter will permit moisture penetration, which will almost certainly result in what is colorfully termed "popcorning," or an explosive rupture of the encapsulant.

In designing power packages, there also are electrothermal thermal-mechanical stresses to consider, Kasem says. "You need to make sure that the device is running at an adequate junction temperature and that you have good materials that can withstand the high junction temperatures," he states. For example, molding compounds can vary widely in their capacity to withstand stress. Although there are several characteristics associated with a good molding compound, one of the most important attributes of plastic packages is the encapsulant's glass-transition temperature. This is the temperature at which the material transitions between a soft, or rubber, state and a solid state.

Molding compounds for high-power devices should ideally have a very high glass-transition temperature to avoid this transition. If the material is experiencing a solid-to-rubber transition as the device undergoes power cycling, this indicates the likelihood of a high thermal mismatch that would apply great strain on the die within the package. That strain is what can cause delamination between chip and plastic and is relieved by either the plastic or the die cracking.

Assuring Integrity

A basic issue for plastic power packages is assuring the package integrity at the plastic-to-metal interface at the point that makes contact with the solder paste. According to Frank LeGeros, senior packaging engineer at Cherry Semiconductor Corp., East Greenwich, R.I., "We see a large potential for mischief to occur at that interface if the proper details are not attended to with respect to mold-compound selection and also the internal design of the package's heat slug."

LeGeros has performed extensive research on the effects of various mold compounds on the integrity of the D^2PAK, a popular SMT variant of the TO-220. His findings indicate that the moisture absorption or permeability characteristics of the mold compound are important factors, but also crucial is the resin system being used. As the D^2PAK and some other SMT power packages are reflow-soldered, the packages' copper header changes temperature much more rapidly than the mold compound, causing differential thermal expansion between the two materials. The resulting shear forces are capable of breaking adhesion between them. In addition, the header's rapid heating can quickly turn any moisture present inside the package into steam, which can rupture the bond between the header and mold compound.

The study led to the conclusion that the choice of mold compound can indeed have a significant impact on the integrity of D^2PAK packages. Among the highest-rated materials was a high-grade biphenol compound. This material had the least observable disbonding between the mold compound and the copper tab when reflowed after a 72-hour, 85°C/85% relative humidity soak cycle. Not faring as well were some general-purpose mold materials, such as a low-stress cresol Novolac thermoset material (common black epoxy). This compound exhibited significant disbonding when subjected to the same conditions as the biphenol compound.

Adhesion of the molding compound can be enhanced by other factors, such as the surface properties of the lead frame itself. Texturing of the lead frame by imposing grooves or dimples to roughen up its surface can give the molding compound more to grab onto, says LeGeros. However, this design technique comes with trade-offs. For example, if the lead-frame surface is

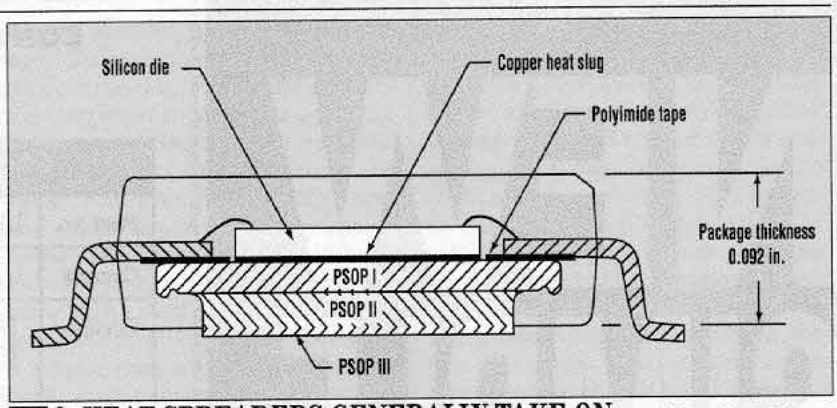
Package	Plastic DIP	Small-outline IC	Power SOP 2	Power SOP 3	TO-220	TO-262	SIP15	PLCC
Enhancing method	Fused leads	Fused leads	Copper slug	Copper slug	Copper header	Copper header	Copper header	Fused leads

1. SHOWN ARE SOME EXAMPLES of thermally enhanced packages for power devices in use at Harris Semiconductor, Melbourne, Fla. Enhancements range from fused leads to copper slugs and headers.

heavily textured, you reduce the area that's available for substrate-to-heat-slug wire bonds. Another factor that can influence molding-compound performance is the decision to plate the entire surface of the internal heat slug or to selectively plate its surface.

One possibility for improvements to the molding compounds is the incorporation of thermally-conductive fillers. According to Maury Rosenfield, senior manager of IC plastic packaging engineering at Harris Semiconductor, Melbourne, Fla., such fillers can provide a 4X to 5X improvement in thermal conductivity. These fillers might consist of substituting aluminum nitride for some of the silica content in the molding compound. Rosenfield says that the use of thermally-conductive fillers doesn't qualify as a true high-power dissipating technique, but is an interim step before resorting to more extreme techniques involving heat slugs and spreaders.

The die-attach material itself also has a glass transition temperature. According to Temic/Siliconix's Kasem, most of today's die-attach materials are made of silver-filled epoxy. These materials can experience a chemical breakdown at elevated temperatures if the glass-transition temperature of either the molding compound or the epoxy is exceeded. As a result, reliability suffers. Die attach traditionally has been performed with soft solder, says Cherry's LeGeros. But LeGeros is impressed with some of the epoxy die-attach materials that have arrived on the scene in recent years and feels that in some cases, they are pushing the thermal properties of the metallic solders.



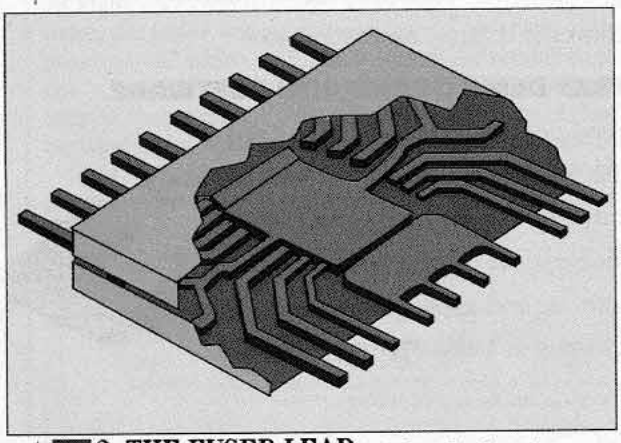
3. HEAT SPREADERS GENERALLY TAKE ON one of three forms. In one, the heat spreader, which is usually in the form of a copper slug, is completely embedded within the package (PSOP I) and is not detectable from the outside. A second type has a slug that is flush with the plastic surface of the SOIC body (PSOP II). The third heat-spreader variant is a slug that actually protrudes from the encapsulant and is very close to the surface-metal plane of the leads. That slug can be soldered directly to the pc board for additional heat sinking (PSOP III).

Lead frames are the subject of a great deal of activity in power packaging. Thermal enhancements of lead frames have enabled some packages traditionally used for discrete power semiconductors to gain new life as IC packages. At Harris Semiconductor, for example, the TO-220-style package has evolved out to 15, and even 23, leads *(Fig. 1)*. "We call that the genesis of the discrete package," says Harris's Rosenfield. Harris uses gold internal wirebonds for the ICs instead of the heavy aluminum wires typically used in discretes. The trade-off there is that the aluminum can handle higher currents, so sometimes heavier or multiple gold wires are used. But the result is that what has historically been known as a discrete package can be pressed into IC service.

The use of discrete packages for ICs is achieved through use of an escalating hierarchy (in terms of cost) of lead-frame and overall package thermal enhancements. First is conversion to an all-copper, lead-frame process. This can be a challenge, according to Dennis Monticelli, vice president of power-management business at National Semiconductor Corp., Santa Clara, Calif. The challenge can be in maintaining the package's reliability and imperviousness to moisture. At Siliconix, additives such as zirconium are used along with the copper in lead frames to create alloys. The resulting material has higher mechanical strength but retains the superior thermal conductivity that copper brings to the party, according to Temic/Siliconix's Kasem.

The next level of enhancement involves the physical design of the lead frame itself. The idea here is to achieve a more direct passage of heat from the die-attach paddle, or the large area to which the die itself is affixed, to the leads. For one, the lead-frame material must be thick enough to handle the power density. Power dissipation is a function of the lead frame's cross section, says Kasem. At the same time, the material must be thin enough to accommodate the requirements of small-size SMT packaging. The typical lead frame is about 4 to 8 mils in thickness, but Siliconix uses up to 10-mil-thick alloys in its custom lead-frame designs.

One technique that has served well at Harris Semiconductor is the use of the "fused" lead frame *(Fig. 2)*. This refers to leads that are fused to the die-attach paddle to provide a direct thermal path from the paddle to the



2. THE FUSED-LEAD technique for thermal enhancement refers to leads that are fused to the die-attach paddle to provide a direct thermal path from the paddle to the pc-board's copper. The trade-off with using fused leads is that each one costs an I/O pin.

pc-board's copper. The trade-off with using fused leads is that each one costs an I/O pin. They're created during fabrication of the lead frame and are at a common potential, which is that of the die-attach paddle. So while the fused leads may cost the package designer I/O, they give him a very effective means of funneling heat away from the die and into the pc board. There are cases, says National's Monticelli, where the IC's I/O needs rule out use of tactics such as fused leads.

Other thermal-enhancement techniques related to the lead frame include enlarging the size of the die-attach paddle. Package designers also will sometimes narrow the distances between the paddle and the leads to form multiple, short thermal-conduction paths through the plastic so that all of the leads, whether dedicated to I/O or not, can participate in channeling heat away from the die.

In terms of package cost and complexity, incorporation of a heat spreader makes for the largest leap *(Fig. 3)*. Heat spreaders generally take on one of three forms. In one, the heat spreader, usually in the form of a copper slug, is completely embedded within the package and is not detectable from the outside. Its task is to uniformly distribute the heat within the package, thus avoiding the formation of "hot spots." A second type has a slug that is flush with the plastic surface of the SOIC body. This type of package is exemplified by the PowerSOP 2 package produced by Amkor Electronics Inc., Chandler, Ariz.

The third heat-spreader variant is a slug that actually protrudes from the encapsulant and is very close to the surface-metal plane of the leads. That slug can be soldered directly to the pc board for additional heat sinking. This also is exemplified by Amkor's PowerSOP 3 package.

Heat-spreader packages are described by Harris's Rosenfield as "true power-IC-type packages." These packages "really maximize thermal dissipation,", he says. "But you have to sacrifice things like cost and board assembly." Still, in Rosenfield's mind, the heat-spreader packages give designers a true high-power-dissipation package that will eventually replace the workaround-type packages represented by TO-220s with extra leads.

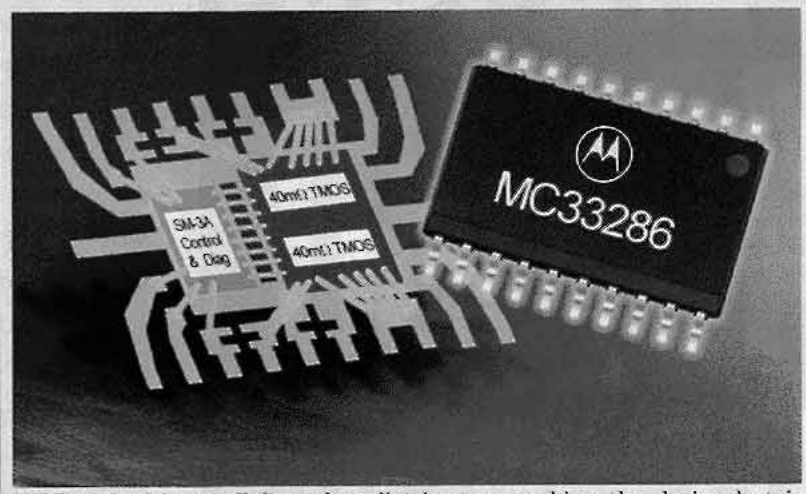
Overall, says Charley Hewitt, director of packaging assembly and technology at Harris Semiconductor, users can expect certain gains from each thermal

MULTICHIP MODULES ENTER POWER FRAY

So what do you do if a particular power-control function is best suited for two separate die, but the customer wants only one package? Well, if you're the Power Products Division at Motorola, Phoenix, Ariz., you put both die into a multichip module. That's what happened when the division came up with its dual high-side driver, which is intended for automotive applications as a replacement for electromechanical relays.

"From the manufacturing point of view, it's more efficient for us to separate the functionality of the power device and the analog device into two pieces of silicon just because the processing for the two technologies is different," says Marty Pandola, product engineer. Manufacturing was more cost-effective that way, and cost is paramount in automotive applications.

But the customer in this case *did* want only one package. So the decision was made to package the dual driver in an SO-20 SMT package, which is a 20-lead small-outline type *(see the photo)*. To accommodate the current within the MCM, a custom lead frame was used with additional wire bonds to the die. Multiple pins are used for the source and drain in each of the device's two 40-mΩ



FETs (wired in parallel) so that all of the devices' current isn't routed through a single pin.

One important element in this device (part no. MC33286BW) is its $R_{DS(on)}$ specification. Another key factor is a good thermal path from the back of the die to the lead frame. It was also crucial to electrically isolate the power device from the analog device. To accomplish that, two different epoxies were used for die attach. Both epoxies are thermally conductive, but the one used to attach the analog die is electrically non-conductive. In the power device, the source leads are on top of the die and the drain leads are on the bottom, making the drain electrically common with the lead frame. Therefore, the die-attach epoxy used for the analog die had to be non-conductive so that the drain of the power FETs wouldn't be tied to the bottom of the analog device.

Cost considerations also dictated that this device, referred to as the Gemini MCM, carry more functionality than its discrete relay equivalents would. These functions include reporting the status of the load (such as whether it's open or shorted), whether the device itself is overheated or seeing an overcurrent condition, and other information back to the CPU.

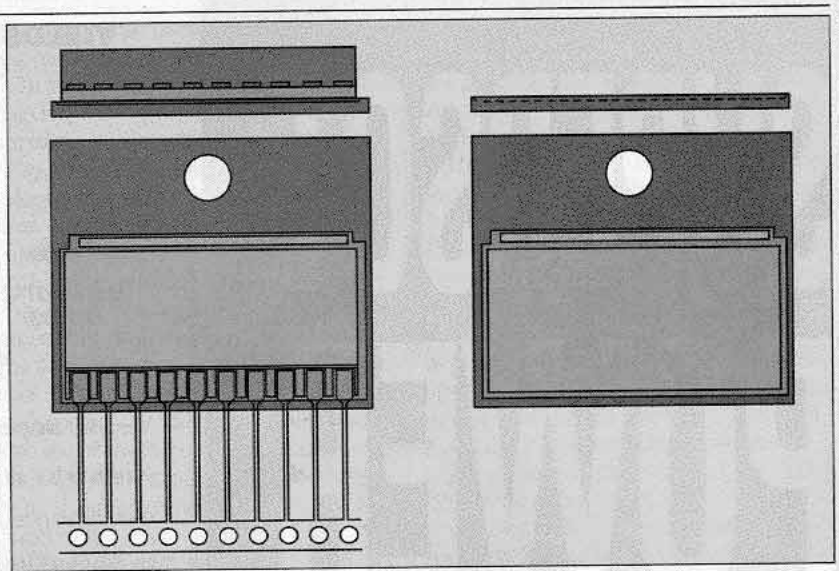
enhancement applied to their power packages. From fused leads, one might expect a 20 to 35% improvement in thermal performance. That figure could be enhanced further if those fused leads are connected directly to heat sinks at the board level. Drop-in heat spreaders give a nominal improvement of about 15 to 30%.

The advent of the heat-spreader package represents the optimum in power dissipation because the die is mounted directly on the slug and the slug can be attached directly to the board. There's no lead-frame interface, which means that there's one less set of thermal resistances to overcome. In a heat-spreader package, he explains, "we mount the IC directly to the slug and can connect that slug to an external heat sink to effectively take advantage of the junction-to-case resistance and lower it considerably."

Another aspect of the heat-spreader package, according to National's Monticelli, is that when they come into play, the burden is placed on the end user to find a way to conduct the heat from the spreader into the board or other heat sink. This effectively makes the user a large part of the thermal-management process.

When the package is installed in its end environment, namely the pc board, the issue becomes one of how well heat is propagated from the device into that environment. This, says Monticelli, is where the semiconductor manufacturer must educate the designer on techniques he or she can use to achieve that goal. If the package has no copper slug and is a basic copper lead-frame package, heat transfer is a matter of how much area of copper foil will be attached to the leads, and in particular to those leads that are connected directly to the lead frame. "You'll see lots of data sheets assuming that an IC is surrounded by a field of copper with data on what kind of thermal performance you can expect for so many square centimeters of copper. That's all well and good for a data sheet, but for today's highly populated boards, that's just not reality," says Monticelli. All too often, reality is a densely populated board and power ICs without much copper connected to the leads.

It's in precisely these kinds of situations where the semiconductor vendors can help customers get the most out of their power-IC packages. There are various techniques that can be used in the board's layout, such as including thermal vias that extend into the copper backplane of a multilayer board. Such techniques, when properly employed, can be a lifesaver, Monticelli says. Such gambits are being used more often by savvy board designers to beat the thermal crunch.



4. IN ITS 10-PIN POWER SIP HYBRID PACKAGE, Apex addresses customer needs for low cost. The package, which is designed to be easy to manufacture with little or no NRE charges, handles watt densities in the neighborhood of 85 to 90 W as well as high voltage and current requirements. It offers a standard SIP outline and resembles an ordinary SIP package.

Across The Board

But in general, designing boards as an environment for ICs with an eye toward thermal concerns is no longer a domain exclusive to designers dealing with power ICs. Power consumption is rising even for ICs in the small-signal realm, which is one reason why semiconductor vendors are pushing so hard to develop low-voltage versions of logic ICs. "These small-signal ICs are getting hot too, and they're in smaller packages, and they have the same kinds of problems that power ICs do," says Monticelli. As a result, thermal management of boards is becoming a normal part of the board-designer's world. There is, in Monticelli's view, a growing awareness in the design community of the need to take a more hands-on approach to thermal management in board design.

The world of power devices is, of course, not limited to ICs. There are many packaging challenges in the field of power hybrids as well. But for hybrids, according to Phil Lehman, manufacturing engineer for the power-amplifier team at Apex Microelectronics Inc., Tucson, Ariz., the big issue is cost. "In many cases, materials costs for the overall hybrid package can be as much as half the total cost of the part," Lehman says. Customers are demanding hybrid packages that can be handled by automatic-assembly equipment, and they want them to have standard package footprints and pinouts so that they can use their existing test sockets.

Apex has come up with a power SIP (single in-line plastic) hybrid package that addresses customer needs for low cost *(Fig. 4)*. Designed to be easy to manufacture with little or no NRE (non-recurring engineering) charges, the package handles watt densities in the neighborhood of 85 to 90 W as well as high voltage and current requirements. It offers a standard SIP outline and, at first glance, resembles a run-of-the-mill SIP package. But a typical SIP package, with its power-handling capacity of perhaps 10 to 15 W, can't measure up to Apex's newest offering.

Achieving this kind of power handling in a SIP required some rethinking of materials. The package's base

material is ceramic and it will have a lid of either ceramic or plastic. Its metal backing will be of either tin-plated nickel or cold-rolled steel. According to Lehman, nickel is better from a thermal standpoint, but its higher cost relative to steel will probably mitigate against its use. Another materials issue was the thickness of the package's lead frame. Most SIPs have lead frames that are 8 to 10 mils in thickness. Apex's power SIP will have a 20-mil-thick lead frame that will handle from 5 to 10 A per pin.

The 10-pin power SIP is slated to carry some existing parts that are now offered in TO-3 packages. In addition, Apex is readying a 14-pin version of the power SIP that's expected to house forthcoming amplifier designs.

Larger power hybrids are also seeing some changes in packaging strategy that also are based on cost. At Motorola's Hybrid Power Modules Group, Phoenix, Ariz., hybrids are looked at as loosely falling into two groups, says Dave Gilbert, the group's operations manager. Customers who purchase hybrids at the low end of the power spectrum, which ranges up to roughly 5 kW, place their emphasis on cost. On the high end, performance is the key element at *any* cost.

For the low-power hybrids, Motorola is planning a family of products that all have a dual-in-line pinout with standard spacing. The idea is to offer customers semi-custom functionality within a generic family of packages *(Fig. 5)*. By changing the substrate internally and altering its pc traces, Motorola will be able to offer almost any electrical function as long as the parts for the function the customer wants will fit.

Estimated dimensions for the packages range from about 2 in. long by 1 in. wide up to about 4 in. long by about 2.5 in. wide, Gilbert says. While the footprint changes, the thicknesses remain essentially the same. Pin spacings and lengths are standardized as well, and pin counts run from 12 up to 26 initially. The company's manufacturing operation is set up for flexibility, and there are plans afoot to place various combinations of die within these generic packages, including MOSFETs, IGBTs, and rectifiers.

Simplicity Itself

A key element to the hybrid package is that it's fairly straightforward and simple. The package housing is a molded plastic housing that incorporates the leads. The substrate is an insulated-metal substrate (IMS), which consists of an aluminum plate with a thin layer of epoxy-type material and then a patterned copper-foil layer on top. Typical pc-board techniques are used to pattern the copper foil. The aluminum plate serves as a heat spreader. Automatic-assembly equipment attaches die to the substrate using solder die-attach techniques and the substrate is mounted in the plastic housing. Then wire bonds are made from the die to the copper foil on the substrate and from the foil to the pins. A sealant is applied to coat the die providing breakdown-voltage protection, and the housing is capped. So ultimately, the modules' electrical configuration relates to substrate and wire-bond patterning.

The first "standard" product in the new package is a 15-A, 600-V six-pack integrated power stage with six IGBTs in a three-phase inverter configuration (part no. MHMP-6B15A60D). The generic package and Motorola's flexible manufacturing capability will enable the company to add specialized functions to that basic module. "Customers often say they'd like us to put some thermal sensing on that substrate. Or maybe they want a seventh switching function for active motor braking. They sometimes want a three-phase-input rectifier bridge in the same circuitry. We can do that in a little larger package," says Gilbert. All of these functions, and others, can be done in any combination.

Beyond the standard IC and hybrid packaging, more exotic packaging techniques such as multichip modules are finding their way into use for power devices *(see "Multichip modules enter power fray," p. 46)*. The industry is always pushing for miniaturization, but miniaturization is at odds with the increasing power requirements of systems overall. It creates real headaches in terms of reliability as well. According to Temic/Siliconix's Mohammed Kasem, the future of power packaging may lie in ball-grid-array, flip-chip, and chip-scale packages. "Reliability, miniaturization, and higher power dissipations are at once the three technology trends and challenges dictating a move toward area-array and chip-scale packages (CSPs) that give you more contact points with the board," Kasem says. Siliconix is actively considering CSPs and flip-chip packages as means of dealing with the power-dissipation and miniaturization requirements, he adds. □

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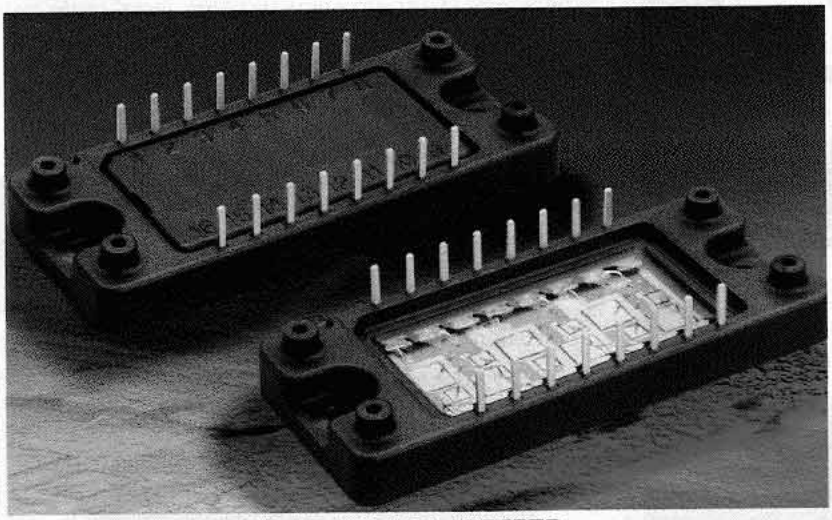

5. THIS EXAMPLE OF A STANDARDIZED hybrid package enables Motorola to offer semi-custom functionality within a generic family of packages. By changing the substrate internally and altering its pc traces, almost any electrical function can be provided as long as the parts for the function will physically fit inside the package.

How Valuable?	Circle
Highly	543
Moderately	544
Slightly	545